Test ROM for Zaccaria 1B1165 CPU Board

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David Gersic http://www.zaccaria-pinball.com

Introduction

One of the challenges to working on an unknown CPU board is that Zaccaria's software diagnostics assume that the board is booted and running. They offer no help in figuring out what is keeping the board from booting. Additionally, due to the hardware design, if anything goes wrong, the board reboots, making testing it somewhat more difficult.

Leon (http://www.flipper-pinball-fan.be) released test ROMs for Zaccaria's 1B1110 (1st Generation) and 1B1165 (2nd Generation) boards a few years ago, along with documentation on how to use them to help diagnose and test a board. These are useful, but in using them, and over the years of repairing many of these boards, I decided that more capabilities were needed.

Hardware Configuration

Minimally, a 1B1165 CPU board, and a power source for +5V and Ground are needed. In order to fully verify that the CPU is working, however, it is helpful to have a testing setup with more capabilities. I have tried to design this to work with a minimal test setup, but the more you are able to supply, I have tried to take advantage of the additional capabilities to make things easier and better.

Power Supply – Using a standard PC power supply for +5 and Ground will work. But using a real Zaccaria 1B1165/0 power supply board and transformer allows testing the POWER FAIL circuit and use of the displays as well.

Inputs – A clip lead with a bit of wire to act as a probe is sufficient. I built a test probe with an alligator clip on one end of a meter probe from a discarded multimeter.

Outputs – Minimally, a few LEDs, with 470 ohm current limiting resistors, and a power supply for them will allow testing the outputs. But, much more is possible using a real 1B1166 Driver Board to test the outputs at CN12, and an eight digit display (1B1168 or 1B11150/0) for CN14.

As with Leon's test setup, initially a jumper is needed to disable the hardware watchdog circuit that reboots the board if it is not running correctly. Connect one end of a clip lead to +5V, and the other end to CN11 pin 8.

Also as with Leon's test setup, connect a LED in series with a 470 ohm resistor. Connect

one end of this to +5 (use the banded end of diode D4 on the CPU board) and the other to the left leg of resistor R111. This is “LED2”. “LED1” is the LED that is on the CPU board.

Burn the image for ROM1 to a 2764. Burn the image for ROM2 to a 2764. Jumper the board for 2 x 2764 (A/B/C/F and H/Y/K/L and J13) and install the ROMs in sockets IC1 and IC2.

If available, connect the power supply to CPU CN9, and Driver to CN13. Connect the ribbon cable between the CPU and Driver boards. Connect the ribbon cable from the CPU to a display.

Turn off all DIP switches on SW1.

Startup

With the watchdog enabled (disconnect the clip lead from CN11 pin 8), turn the power on. A logic probe, or oscilloscope on TP4 should show a signal cycling High / Low about two times a second.

Disable the watchdog by connecting the clip lead at CN11 pin 8. The board should boot and begin running. Confirmation of bootup:

1. LED1 and LED2 should come on
2. LED1 and LED2 go off
3. LED1 blinks twice
4. LED2 blinks twice

This confirms that the board is booted and running. Minimally, that means that the 2650 processor is ok, ROM1 is readable (so chip select is working) and LED1 and LED2 are working. If a display is connected, it will flash on and off along with LED1, and should be displaying all digits 0.

If the board does not start:

1. Check to make sure that the clock circuit is running (TP2) and reaching the CPU at pin 38 correctly.
2. Check to make sure that +5V and Gnd are reaching the CPU and ROMs and other chips correctly.
3. Check IC8 and IC17, since they control the Chip Select circuit.
4. Check to make sure that there are no broken traces on the Address or Data Bus lines between the CPU, ROM1, and the pullup resistors at R2...R9.

Next, the startup code tests the inputs that will be needed for everything else.

SENSE

1. Display 5 (Ball / Credit) will go blank, and a 5 will be displayed in the left-most digit.
2. LED1 and LED2 will begin blinking on and off
3. Using a probe wire connected to Ground, connect the other end to TP1
4. LED1 will stay on, LED2 will continue blinking, and a 5 will be displayed in the right-most digit of Display 5.
5. Remove the wire from TP1
6. Both LED1 and LED2 will turn off and the test pauses for approximately 2 seconds.

DIP Switch 1

1. LED2 will blink twice
2. LED1 will come on
3. The digits “51” will be displayed in the left-most two digits of Display 5.
4. LED2 will begin blinking on and off
5. Turn on SW1 on the DIP Switch bank
6. LED2 will come on and stay on
7. Turn off SW1
8. Both LED1 and LED2 will turn off
9. After a pause of approximately 1 second, LED1 will come on again
10. Turn on, then off SW2, SW3, and SW4. Each one will be confirmed.

After confirming that LED1, LED2, SENSE, and the four DIP switches are working, the main test loop starts. LED1 and LED2 will be flashing, alternating between them. Select a test using the DIP switches, and start it by grounding TP1.

Display 5, if connected and working, is used to make the startup tests a little easier to follow. They can only display digits 0-9, so a “5” is used in place of an “S”. For the SENSE line test, “5” (“S”) in the left-most digit shows what the test is waiting for, and a “5” (“S”) in the right-most digit confirms that it has been read successfully. For the DIP Switch tests, “51” is “S1” for “Switch 1”, followed by “52”, “53” and “54” (“Switch 4”) to show which one is being tested at the time.

Test Selection

Each test can be selected in any order from the main loop. Once a test completes, it will signal success or failure, then return to the main loop.

Test 1	SW1	Inputs Test
Test 2	SW2	Outputs Test
	SW2 & SW1	Outputs Test 2
Test 3	SW3	ROMs Checksum Test
	SW3 & SW1	ROM1 Checksum Test
	SW3 & SW2	ROM2 Checksum Test
Test 4	SW4	RAM Test
	SW4 & SW1	RAM Test – Continuous Loop

Test Description: Inputs

Turn on SW1 on the DIP switch bank, and ground TP1 to start the inputs test.

LED1 will be turned on, and the test starts.

Using a probe connected to ground, touch each of the input pins on CN11 (pins 10, 11, 12, 13, 14, 15, 16, 18).

For each input, LED2 will flash indicating which input was grounded (pin 10 = 1 flash, pin 11 = 2 flashes, pin 18 = 8 flashes).

If more than one pin is grounded, or if there is a problem reading the inputs, then the wrong number of flashes may be counted. Additionally, the 8 digit display is used to show which input(s) are grounded. Display digits showing 0 are open, 1 are closed. This provides a quick and easy way to see more than one input being closed.

The four input pins from the Sound Board on CN8 (pins 20, 19, 18, and 17) can also be tested by grounding them. LED2 will double-flash to indicate these, and they will also be displayed on the 8 digit display.

This test loops until SW1 is turned off, then returns to the main test program loop.

Test Description: Outputs

Turn on SW2 and ground TP1 to start the outputs test.

The CPU has multiple sets of outputs to be tested. This test loops through the five sub-tests described below.

Outputs Test: CN14 – Displays

With a display connected to CN14, the digit displays will cycle through the digits 0...9.

Without a display connected, a logic probe or 'scope can be used to check the output pins on CN14 (pins 8, 7, 10, 1, 4, 3, 6, 9, 12, 11, 14, 13, 16) for activity.

Outputs Test: CN12 – Solenoids

With a Driver Board connected, the 24 solenoids are cycled on/off. Starting with Q1, Q3, Q5, Q6, Q8, Q10, Q11, Q13, Q15, Q16, Q18, Q20, Q21, and Q23 turned on, then alternating between these and Q2, Q4, Q7, Q9, Q12, Q14, Q17, Q19, Q22, and Q24. I have these permanently connected to a +5V power supply, LED, current limiting resistor, and CN14 on a driver board, so that it is easy to watch them flash on and off. A single test LED, or a logic probe, can be used to check the outputs via the Driver board.

Without a Driver board connected, watch for activity with a logic probe or oscilloscope at CN12 pins (pins 18, 19, 20, 4, 3, 6, 7, and 8).

This test loops through the alternating cycle 5 times.

Outputs Test: CN12 – Lamps

This test is similar to the Solenoids test, described above, but now alternating between the 80 lamp SCRs. Starting with the odd numbered LEDs (1, 3, 5, etc.) turned on, then switching those off and turning on the even numbered ones. As with the Solenoids test, this is easiest with a Driver board and some permanently connected LEDs, but a logic probe or oscilloscope will work as well.

Without a Driver board, watch for activity with a logic probe or oscilloscope at CN12 pins (pins 18, 19, 20, 4, 3, 1, 2, 9, 10, 11, 12, 13, 14, 15, 16).

This test loops through the alternating cycle 5 times.

Outputs Test: CN8 – Sound Board

The 10 output lines to the sound board at CN8 are alternately cycled on and off.

A permanent connection of some test LEDs to pins (2, 4, 8, 12, 16, 14, 10, 6, 11,

15) of CN8 with current limiting resistors is ideal. A logic probe or oscilloscope can be used as well.

This test loops through the alternating cycle 5 times.

Outputs Test: CN10 / CN11 – Switch Matrix

There are eight output lines that drive the switch matrix when the CPU is normally running in a game.

Connect a test LED to CN10 pin 6 and each of pins (2, 3, 4, 5, 6, 7, 9) on CN11.

This set of outputs is different from the others in that one of them is always on. For this test, the test cycles through all 8 possible values.

Ideally, connect 8 test LEDs, one to each line, and watch it cycle through them.

The outputs test will then loop back to the Displays test, repeating all of these until SW2 is turned off.

Test Description: Outputs 2

Turn on SW2 and SW1 and ground TP1 to start the outputs test.

The CPU has multiple sets of outputs to be tested. This test loops through the five sub-tests described below. All outputs are tested simultaneously in this test.

Outputs Test: CN14 – Displays

With a display connected to CN14, the digit displays will cycle through the digits 0...9.

Outputs Test: CN12 – Solenoids

With a Driver Board connected, the 24 solenoids are cycled on/off. Starting with Q1, Q3, Q5, Q6, Q8, Q10, Q11, Q13, Q15, Q16, Q18, Q20, Q21, and Q23 turned on, then alternating between these and Q2, Q4, Q7, Q9, Q12, Q14, Q17, Q19, Q22, and Q24.

Without a Driver board connected, watch for activity with a logic probe or oscilloscope at CN12 pins (pins 18, 19, 20, 4, 3, 6, 7, and 8).

Outputs Test: CN12 – Lamps

This test is similar to the Solenoids test, described above, but alternating between the 80 lamp SCRs. Starting with the odd numbered LEDs (1, 3, 5, etc.) turned on, then switching those off and turning on the even numbered ones.

Without a Driver board, watch for activity with a logic probe or oscilloscope at CN12 pins (pins 18, 19, 20, 4, 3, 1, 2, 9, 10, 11, 12, 13, 14, 15, 16).

Outputs Test: CN8 – Sound Board

The 10 output lines to the sound board at CN8 are alternately cycled on and off.

Outputs Test: CN10 / CN11 – Switch Matrix

There are eight output lines that drive the switch matrix when the CPU is normally running in a game.

Connect a test LED to CN10 pin 6 and each of pins (2, 3, 4, 5, 6, 7, 9) on CN11.

This set of outputs is different from the others in that one of them is always on. For this test, the test cycles through all 8 possible values.

Ideally, connect 8 test LEDs, one to each line, and watch it cycle through them.

This test will run until SW2 and SW1 are turned off.

Test Description: ROM Checksums

To verify that all address and data lines are working between the CPU and the ROMs, and that the chip select logic is able to select the correct ROM, each of the two ROMs installed can be read and its checksum calculated, then compared against stored known-good values.

Checksum Test:

The default checksum test (SW3 on, Ground Sense line to start) is to test first ROM1, then ROM2.

For each test, at the start, LED1 will blink once (on-off-on), then the test starts. The ROM is read in four banks, and LED2 will blink once for each bank as it is being tested. The contents of the ROM are read and the checksum calculated. This checksum is then compared to a stored checksum (in ROM1). If the calculated checksum matches the stored checksum, then LED1 will blink twice, and the test ends. If the calculated checksum does not match the stored checksum, then LED1 will blink nine times (three

fast, three slow, three fast, aka “S.O.S.”), then LED2 will blink once to indicate a failure reading ROM1, or twice to indicate a failure reading ROM2.

After testing ROM1, the test runs again for ROM2.

Alternate Checksum Test:

Because sometimes you may not want to test both ROMs, it is possible to run only the test for ROM1 or ROM2.

To test ROM1, with SW3 and SW1 on, Ground the Sense line to start. The checksum test will run for ROM1 only, then return to the main loop.

To test ROM2 only, with SW3 and SW2 on, Ground the Sense line to start.

Test Description: RAM

There are three RAM chips on the 1B1165 CPU board. IC4, IC5, and IC23. This test is actually three tests, verifying that the address lines and chip select work, the data lines work, and that all memory addresses are readable and writable and able to store and retrieve correct data.

RAM Test 1:

A byte of data is written to the first memory address (0x1800), using a walking-1 pattern. Each write is then verified by reading back what was written. LED1 is turned on to indicate that this test is running.

RAM Test 2:

A byte of data is written to memory at memory addresses testing that each address line is working. LED1 is turned off, and LED2 is turned on to indicate that this test is running.

RAM Test 3:

A walking-1s pattern is written and verified to every possible memory address. Both LEDs are turned on to indicate that this test is running. If you have displays and a driver board connected, you will see some of the outputs go active during this test, as the outputs are actually memory mapped devices.

If the test passes, at the end of test 3, both LEDs will flash two times.

If one of the tests fails, LED1 will flash nine times (“S.O.S.” again), then either LED1 or LED2 will be turned on to indicate whether the failure was in the low order or high order

nybble of the byte that was written. Generally, a low order nybble failure is a fault with IC4, but it could potentially be with IC23 as well, depending on the address of the failure. A high order failure is always IC5.

RAM Test – Continuous Loop:

The normal RAM test (SW4 on) is a single loop through memory, indicates pass or fail, then returns to the main test program loop. If SW4 and SW1 are on, then the test will loop through Test 1, Test 2, and Test 3 continuously until SW4 and SW1 are turned off.

RAM Test – Interrupt Service Routine and the Reboot Watchdog:

At the end of the first successful RAM test, an Interrupt Service Routine is activated. This uses memory, so it requires that the memory test pass before it is allowed to activate. Once active, it uses the board's hardware interrupt to strobe the RFSH line, which keeps the hardware reboot watchdog from forcing the processor to reboot.

Once this ISR is in place, the jumper can be removed from CN11 pin 8. The test should continue running normally. This tests the board's ability to correctly fire and service interrupt requests, as well as its ability to reset the watchdog and keep it from rebooting the board.

Once the ISR is running, further testing using tests 1 (Inputs) and 2 (Outputs) will proceed normally and can be done without the watchdog disable jumper at CN11 pin 8. The ROM checksum and RAM tests, however, require that the watchdog disable jumper be installed, as they disable interrupts while running.

Bugs

1. Changing switches on DIP Switch 1, while the memory test is running, tends to make the memory test fail. I suspect that, since these switches are read from the data bus, that changing them while the test is running is affecting the data on the bus, causing the test to detect a failure.

Credits

Leon
http://www.flipper-pinball-fan.be

Alan R. Baldwin
as2650 cross assembler
http://shop-pdp.kent.edu/ashtml/asxxxx.htm

Michael Barr - Fast Accurate Memory Test Suite
http://www.netrino.com/Articles/MemoryTesting/index.php